Appln. No. 10/718,270
Amendment dated July 30, 2008
Office action of April 2, 2008

PATENT

IN THE CLAIMS

What we claim is:

Claims

1. (currently amended) A method for efficiently processing layers of a data packet, comprising:

defining a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system, the pipeline of processors consisting of multiple separate processors;

receiving a data packet from the distributed network into a first stage of one of the multiple separate processors of the pipeline of processors;

processing the data packet to remove a header associated with the first stage;

transmitting the processed data packet to a second stage associated with another one of the multiple separate processors for processing associated with the second stage;

repeating the operations of processing the data packet and transmitting the processed data packet for successive stages associated with corresponding processors until a header associated with a final stage has been removed from the data packet; and

transmitting the data packet from the final stage to the CPU of the host system.

2. (original) The method of claim 1, wherein the data packet is an Ethernet data packet.

Appln. No. 10/718,270
Amendment dated July 30, 2008
Office action of April 2, 2008

PATENT

3.   (currently amended) The method of claim 1, wherein each processor of

the pipeline ~~of the pipeline~~ of processors includes at least three <u>separate</u> buffers

configured to maintain a line rate<u>, the three separate buffers receiving input from a</u>

<u>common multiplexer</u>.

4.   (original) The method of claim 1, wherein the successive stages

correspond to layers of the data packet.

5.   (original) The method of claim 4, wherein the layers are selected from

the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

6.   (original) The method of claim 1, wherein the method operation of processing

the data packet to remove a header associated with the first stage includes,

defining instructions for processing the data packet; and

enabling an arithmetic logic unit (ALU) associated with each processor to

process the instructions.

7.   (original) The method of claim 6, wherein the method operation of

enabling an arithmetic logic unit (ALU) associated with each processor to process the

instructions includes,

aligning the instructions by a least significant bit; and

extending each of the instructions to a defined bit size.

Appln. No. 10/718,270
Amendment dated July 30, 2008
Office action of April 2, 2008

PATENT

8.   (currently amended) An adapter card configured to be in communication with a general purpose computer, comprising:

a plurality of <u>distinct</u> processors arranged in a pipeline architecture, the plurality of <u>distinct</u> processors defining a receiving pipeline and a transmitting pipeline, each <u>processor</u> of the plurality of <u>distinct</u> processors associated with a pipeline stage, each pipeline stage configured to process a layer of a data packet, wherein the receiving pipeline removes layers from the data packet and the transmitting pipeline adds layers to the data packet.

9.   (original) The adapter card of claim 8, wherein the pipeline stage is associated with a layer of an Ethernet packet header.

10.   (original) The adapter card of claim 9, wherein the layer is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

11.   (original) The adapter card of claim 8, wherein the adapter card is a network interface card.

12.   (currently amended) The adapter card of claim 8, wherein each of the plurality of processors include at least three <u>separate</u> buffers for maintaining an

Appln. No. 10/718,270
Amendment dated July 30, 2008
Office action of April 2, 2008

PATENT

incoming line rate, the three separate buffers receiving input from a common multiplexer.

13.　(original) The adapter card of claim 8, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width so that a pre-extending bit width of the operand is transparent to an arithmetic logic unit configured to process the operand.

14.　(currently amended) A general purpose computer, comprising:

a central processing unit (CPU);

a network interface card (NIC) configured to process data packets, the NIC including,

a plurality of distinct processors arranged in a pipeline architecture, the plurality of distinct processors defining a receiving pipeline and a transmitting pipeline, each processor of the plurality of distinct processors associated with a pipeline stage, each pipeline stage configured to process a header associated the data packets, wherein each of the distinct processors of the receiving pipeline removes headers from the data packets and each of the distinct processors of the transmitting pipeline adds headers to the data packets.

15.　(original) The general purpose computer of claim 14, wherein the pipeline stage is associated with a layer of a header of the data packets.

Appln. No. 10/718,270
Amendment dated July 30, 2008
Office action of April 2, 2008

PATENT

16.   (original) The general purpose computer of claim 15, wherein the layer of the header of the data packets is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

17.   (currently amended) The general purpose computer of claim 14, wherein each of the plurality of processors have at least three separate buffers configured to maintain an incoming line rate, the three separate buffers receiving input from a common multiplexer.

18.   (original) The general purpose computer of claim 14, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width so that a pre-extending bit width of the operand is transparent to an arithmetic logic unit configured to process the operand.

19.   (original) The general purpose computer of claim 14, wherein each of the plurality of processors are configured to execute a two stage pipeline process.

20.   (original) The general purpose computer of claim 14, wherein each of the data packets have a variable packet size.